D0Note 4430

Cabling for the Run IIb L1 Calorimeter Upgrade

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Abstract

During the Run IIb upgrade scheduled for the summer of 2005, the existing Level 1 Calorimeter trigger electronics will be replaced. The existing cables, which provide the trigger pick-off signal from the calorimeter will be reused, but the input to the new electronics will use a different kind of cable and connector, thus, requiring some form of transition connector, patch panel or bulkhead. The layout of the new calorimeter trigger racks and electronic crates should also minimize the movement of the existing and irreplaceable cables. A new map of the calorimeter precision readout and the existing and upgrade trigger readout is presented including physics and trigger channels, racks inside and outside the collision hall, electronics crates and readout cards, and all cables.

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Introduction

The DØ Run IIb upgrade, scheduled for the summer of 2005, will improve the selection of data samples required for the Higgs search and the high-p_T physics program while providing sufficient background rejection to meet constraints imposed by the readout electronics and data acquisition system [1].

The DØ Run IIb trigger upgrade is designed to operate at a peak luminosity of $5x10^{32}$ $cm^{-2}s^{-1}$ with 132 ns bunch spacing. The laboratory baseline plan for Run IIb is a luminosity of $2x10^{32}$ cm^{-2} sec^{-1} with 396 ns bunch spacing, but DØ should have the capability of operating at higher instantaneous luminosities with either bunch spacing. The DØ trigger upgrade is consistent with this plan.

The main elements of the calorimeter trigger upgrade are listed below.

- Analog to Digital Converter and Digital-Filter Boards (ADF) that receive analog Trigger Tower (TT) signals from the Baseline Subtracter (BLS) cards, digitize them, convert from energy to transverse energy (ET) and perform the digital filtering to associate energy with the correct bunch crossing. Each of these boards deals with signals from 16 Electromagnetic Trigger Towers [EM TTs] and 16 Hadronic Tigger Towers [HD TTs].
- ADF Timing Fanout boards that send timing signals coming from the trigger framework to the ADF cards.
- Trigger Algorithm Boards (TAB) that receive TT transverse energies from the ADF boards, produce EM and jet cluster ET's using the sliding windows algorithm and begin the global summing process that will yield scalar summed transverse energy ($E_{T,total}$) and missing transverse energy (Mp_T). Outputs will also be provided at this level for data transmission to L2/L3 and to the Cal-Track Match system.
- A Global Algorithm Board (GAB) that receives data from the TABs and produces the final $E_{T,total}$ and Mp_T, as well as providing an interface to the DØ Trigger Framework and a timing fanout. One Global Algorithm Board (GAB) is required for the system. It will be housed in the same crate as the TABs to facilitate communication between them.

Physical Layout

Run I

The existing L1 calorimeter trigger electronics reside on the first floor of the Moveable Counting House (MCH) occuping 20 crates in 10 racks (Figures 1a-b).

Each rack contains the calorimeter trigger front-end (CTFE) cards for 128 trigger towers TT (all 32 ϕ's for four consecutive η's) as it is shown in Figures 1a-b.

M103 TT η=(+1:+4)
M104 TT η=(-1:-4)
M105 TT η=(+5:+8)
M106 TT η=(-5:-8)
M107 TT η=(+9:+12)
M108 TT η=(-9:-12)
M109 TT η=(+13:+16)
M110 TT η=(-13:-16)
M111 TT η=(+17:+20)
M112 TT η=(-17:-20)

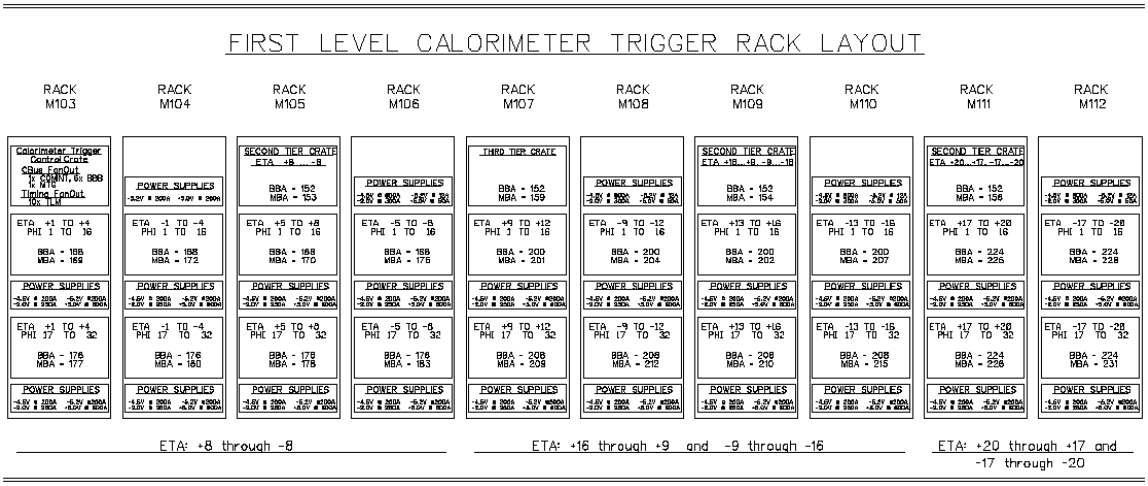

Figure 1a: Diagram of the existing L1 CAL Run I trigger rack layout in MCH1 [2]. There are ten racks – M103 through M112 - each with two crates of electronics .

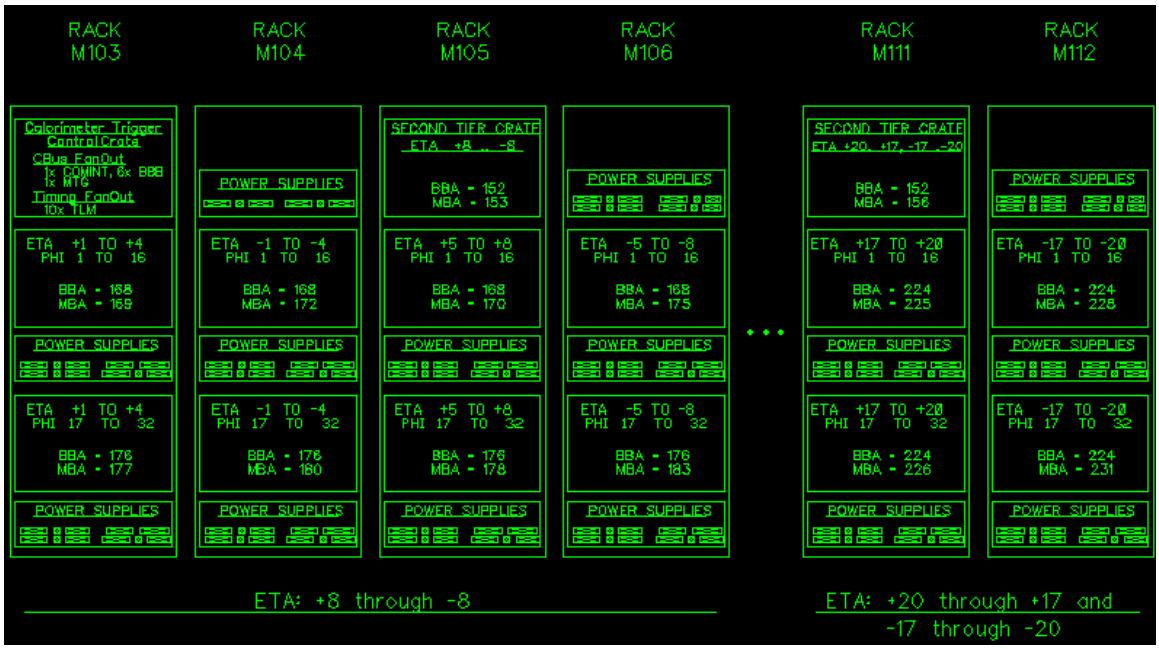

Figure 1b: Diagram of the existing L1 CAL Run I trigger rack layout in MCH1 detail [2]. In each rack, all trigger towers for all phi and a set of four etas are readout.

Run IIb

Run IIb will retain the present trigger architecture with three trigger levels. However, the existing calorimeter trigger electronics will be replaced with a new more compact system. The new electronics will be housed in five 6U VME crates in five racks. The ADF racks will be located in M104, M106, M109 and M111 as shown in Figure 2. The TAB/GAB rack will be located in M107. The remaining rack space can be used for patch panels described below. There is flexibility in the new layout (Figure 2b) to reposition any rack to the right or left by one rack.

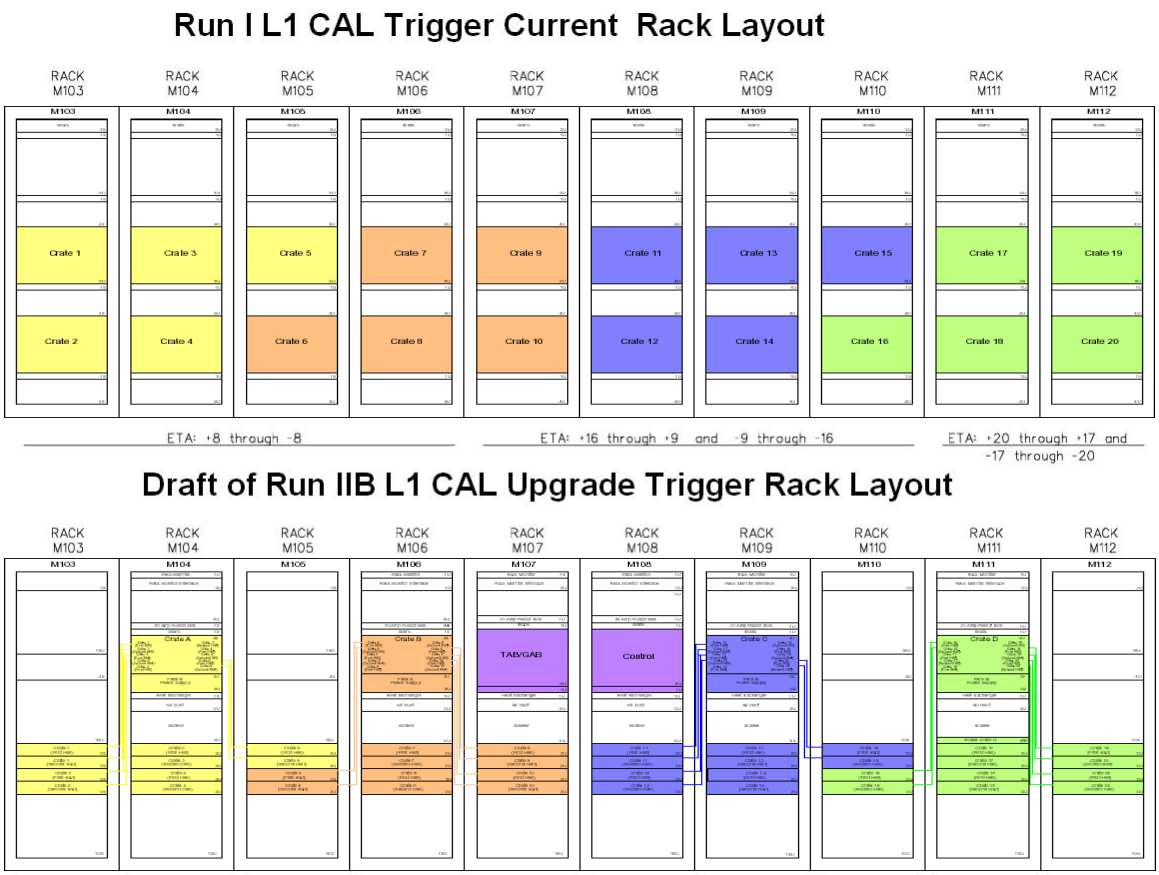

Figure 2: (Figure 2a) Existing and (Figure 2b) proposed calorimeter trigger rack layouts. The color code shows how the calorimeter trigger inputs will be reassigned from the existing trigger crates to the new ADF crates.

Each ADF rack contains only one ADF crate, which contains 20 ADF boards with 16 channels each. Also each channel corresponds to one trigger tower. Each ADF crate and rack receives inputs from 320 TTs.

ADF Rack 1 ("M104") "Yellow".
TT $\eta=(+1:+4)\times\phi$=(1:32) + $\eta=(-1:-4)\times\phi$=(1:32) + $\eta=(+5:+8)\times\phi$=(1:16)

ADF Rack 2 ("M106") "Red"
TT $\eta=(+5:+8)\times\phi$=(17:32) + $\eta=(-5:-8)\times\phi$=(1:32) + $\eta=(+9:+12)\times\phi$=(1:32)

ADF Rack 3 ("M109") "Blue"
TT $\eta=(-9:-12)\times\phi$=(1:32) + $\eta=(+13:+16)\times\phi$=(1:32) + $\eta=(-13:-16)\times\phi$=(1:16)

ADF Rack 4 ("M111") "Green"
TT $\eta=(-13:-16)\times\phi$=(17:32) + $\eta=(+17:+20)\times\phi$=(1:32) + $\eta=(-17:-20)\times\phi$=(1:32)

The ADF boards are labeled from 1 to 80. Boards 1 to 20 are in rack number 1 and so on. The eta & phi distribution per board is shown in Figure 3.

ADF Board – Trigger Eta & Phi Distribution

Trigger Eta vs Phi	Current Rack	1 4	5 8	9 12	13 16	17 20	21 24	25 28	29 32
-17 –20	M112	73	74	75	76	77	78	79	80
-13 –16	M110	57	58	59	60	61	62	63	64
-9 –12	M108	41	42	43	44	45	46	47	48
-5 –8	M106	25	26	27	28	29	30	31	32
-1 –4	M104	9	10	11	12	13	14	15	16
1 4	M103	1	2	3	4	5	6	7	8
5 8	M105	17	18	19	20	21	22	23	24
9 12	M107	33	34	35	36	37	38	39	40
13 16	M109	49	50	51	52	53	54	55	56
17 20	M111	65	66	67	68	69	70	71	72

Figure 3: Eta-Phi distribution per ADF board compared with the current Eta-Phi distribution per rack. Yellow=ADF Rack 1, Red= ADF Rack 2, Blue=ADF Rack 3 and Green=ADF Rack 4.

Level 1 Calorimeter Cabling

Introduction

The new trigger layout will reuse the existing cables, which provides the trigger pick-off signal from the calorimeter platform BLS racks to MCH1. These cables are commonly referred to as “the Blue cables” [3] Figure 4a and were installed at the very beginning of Run I. They are made of 0.1 inch diameter ribbon coaxial cable. Four adjacent coaxial cables in one ribbon are used to carry the differential EM and HD signals for a given trigger tower. This ribbon coaxial cable was made by a company called New England Wire. The lengths of the Blue cables are:

- 130 feet to North End-Cap Calorimeter [EC]
- 150 feet to Central Calorimeter [CC]
- 180 feet to South End-Cap Calorimeter [EC]

The Blue cables are terminated with an 8 pin Amphenol connector at the MCH1 end. The ADF boards require a 20 pin AMP connector, so it is not possible to connect the Blue cables directly into the ADF boards [4]. Extension cables and patch panels to make the transition from the Blue cables to the ADF boards is needed. The design of this signal transition system will be described in a later D0 Note.

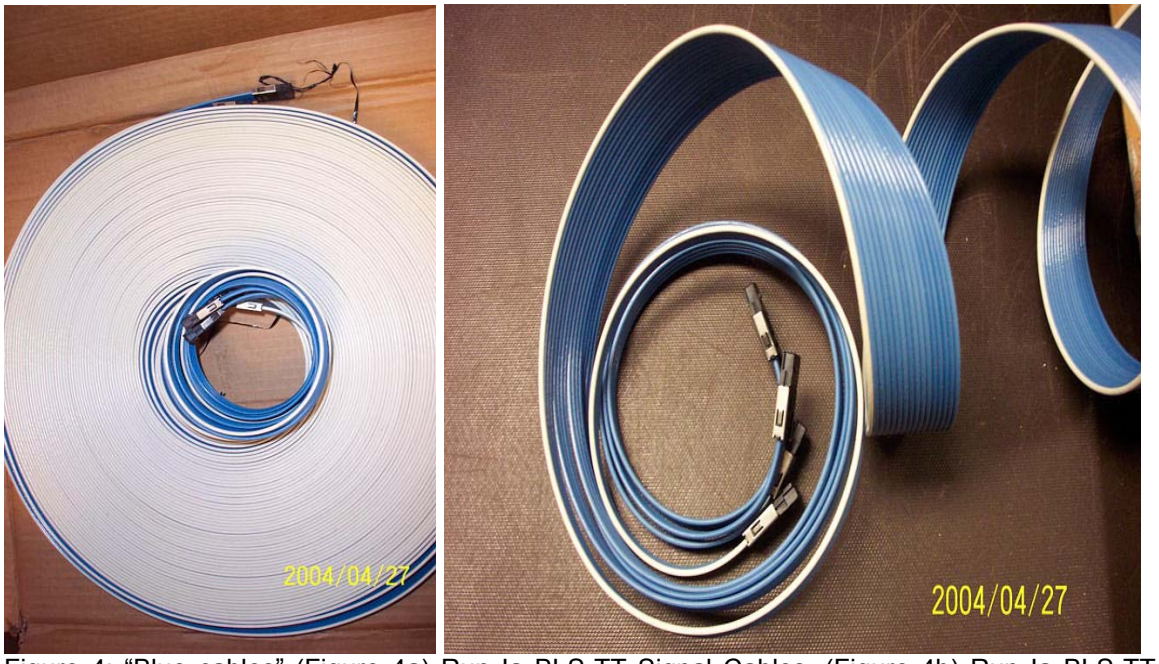

Figure 4: “Blue cables” (Figure 4a) Run Ia BLS-TT Signal Cables. (Figure 4b) Run Ia BLS-TT Amphenol Connectors

There are other advantages to using patch panels for the new layout. The movement of the Blue cables is minimized. The Blue cables cannot be replaced because of their age and their location inside the collision hall. The patch panels make easier accessing the signals and debugging the connections and cables. A design for strain relief and cable flow to ease airflow and cooling will be simpler if the extra racks with patch panels are used.

There are 1280 trigger towers and each trigger tower is comprised of an EM and an HD channel therefore there are 2560 analog channels in total. Each ADF card accommodates 32 channels or 16 TTs each (Figure 5) with an EM and HD component. There are 80 ADF cards in total (Figure 7). The ADF cards are housed in 4 fully populated 21-slot crates. Each crate contains 20 ADF cards and a VME Interconnect to make the interface to the Trigger Control Computer (TCC) Figure 6. There are a total of 320 TTs in each ADF crate, and only one ADF crate in each ADF rack.

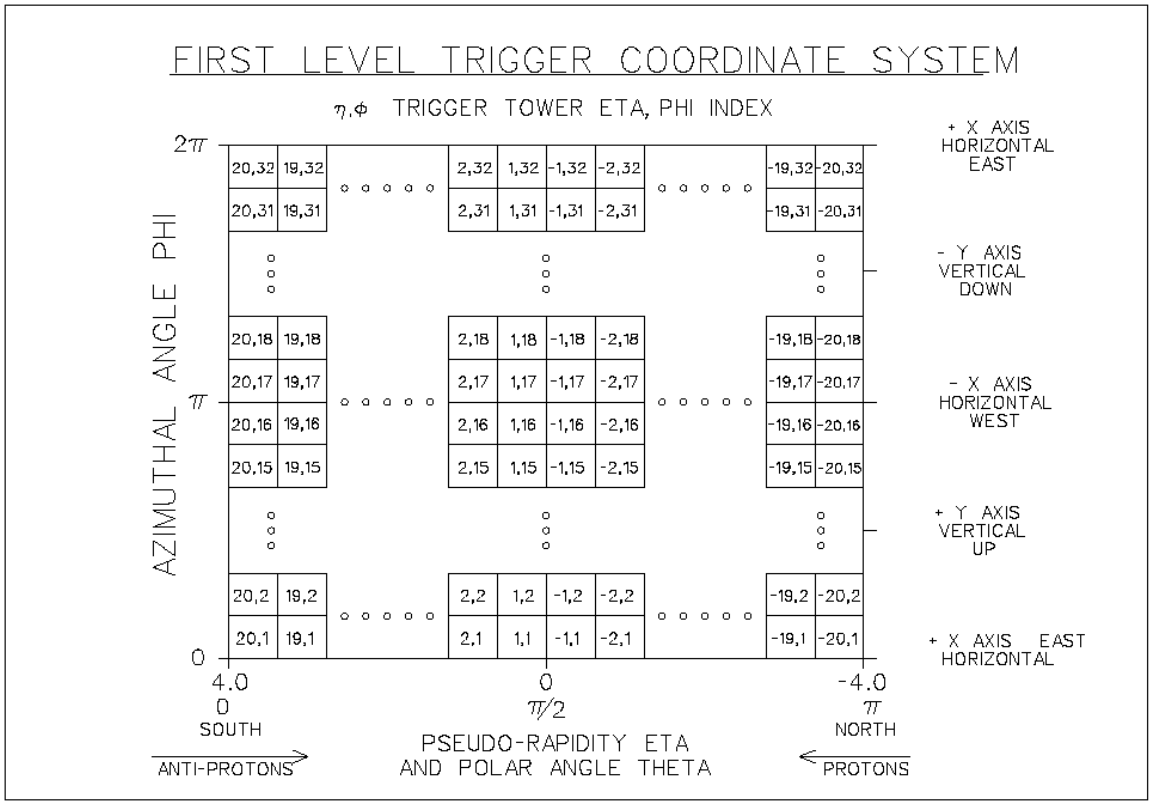

Figure 5: Calorimeter Trigger Tower coordinate system in azimuthal angle, phi, and pseudorapidity, eta. There are 1280 total trigger towers.

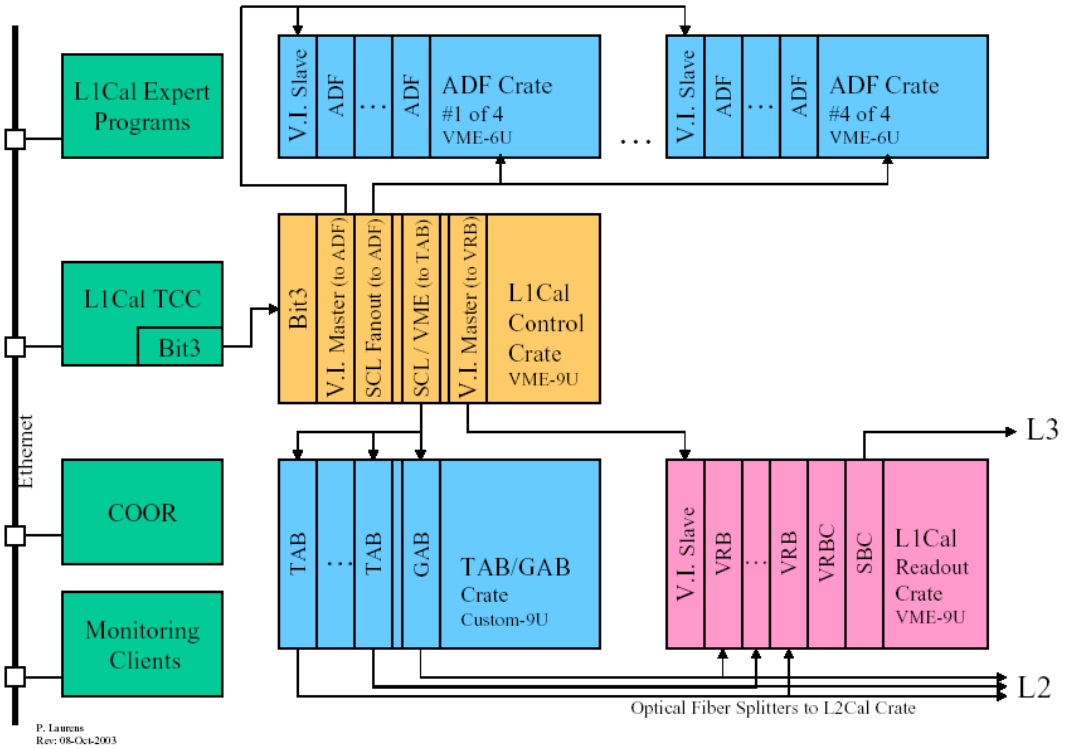

Figure 6: Run IIb L1 Calorimeter Trigger Control Path

There are three output cables from each ADF card (Figure 6) which carry identical copies of the ADF card data (Figure 7). Each TAB card (Figure 8) has ten sliding windows (SW) chips. Each SW chip receives inputs from 3 different ADF cards. A total of 30 cables from ADF cards in each of the four ADF crates with signals from 480 TTs are received by each TAB card as shown in Figure 9. There is a three-fold redundancy in the TT input to the TAB system.

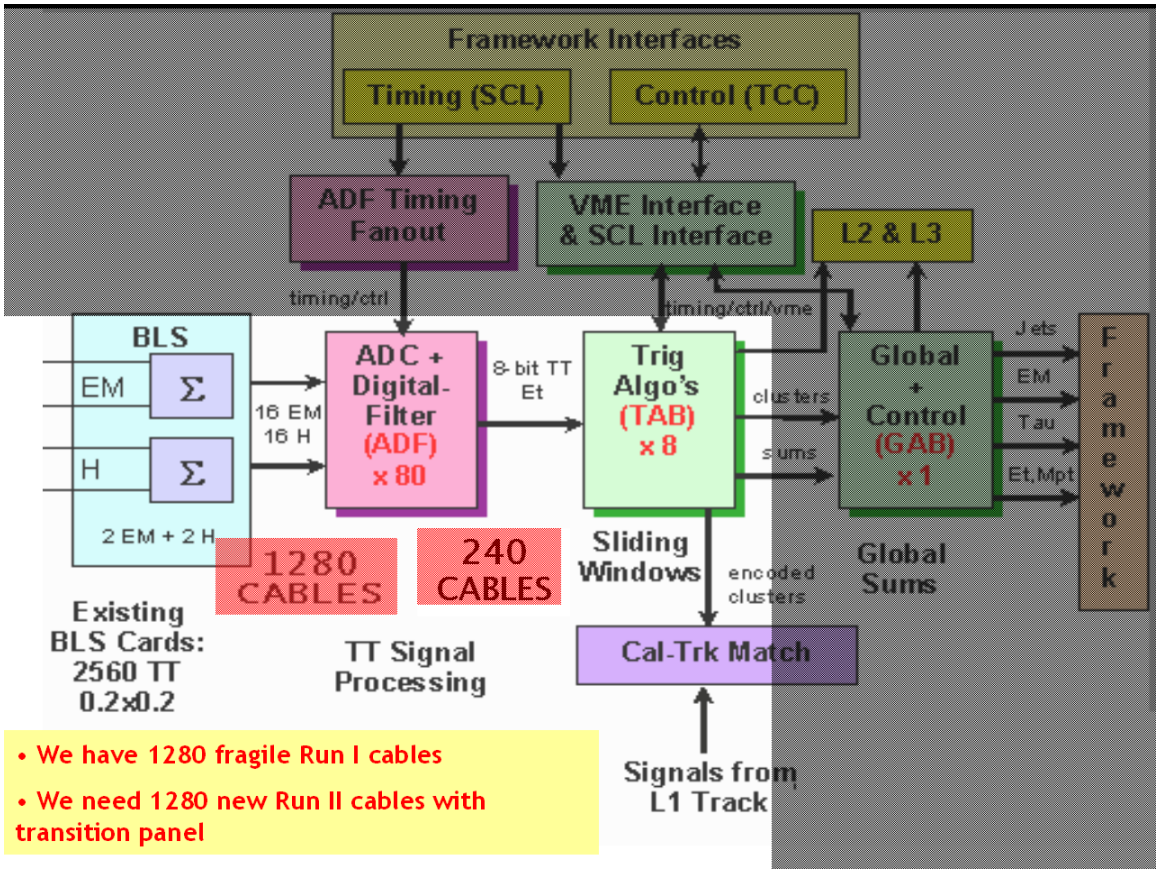

Figure 7. Block diagram of L1 calorimeter trigger system.

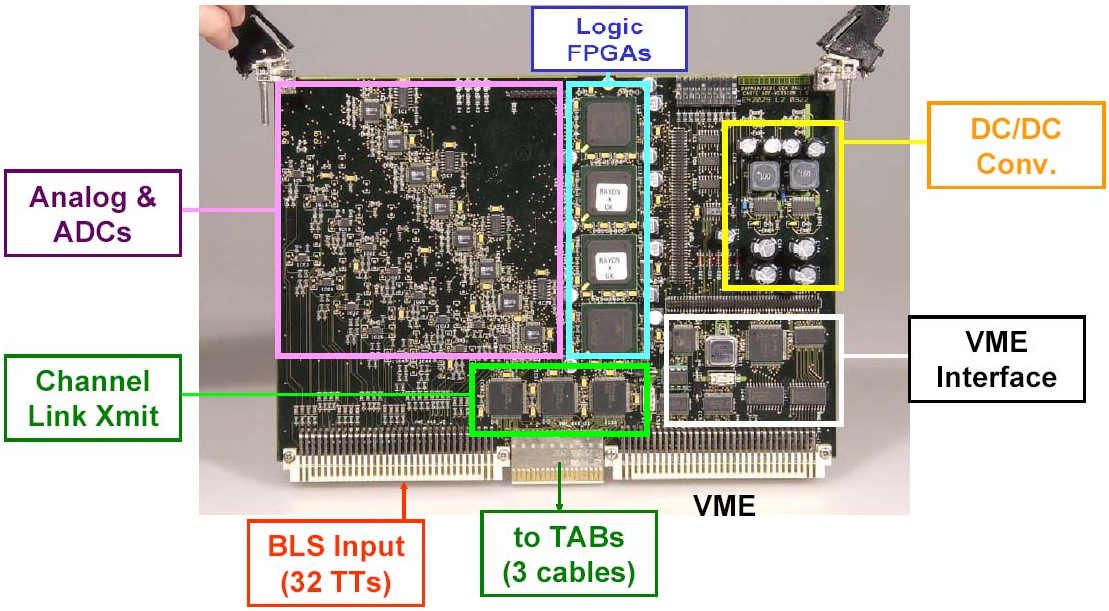

Figure 8: Analog to Digital-Digital Filtering (ADF) prototype which receives inputs from 16x2 Trigger Towers (TTs).

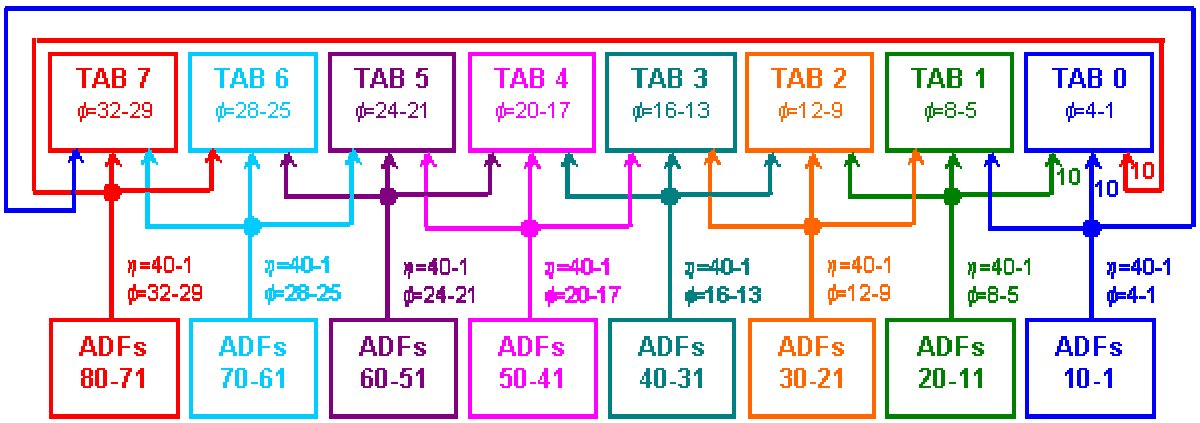

Figure 9: Diagram of signal flow between the ADFs and the TABs.

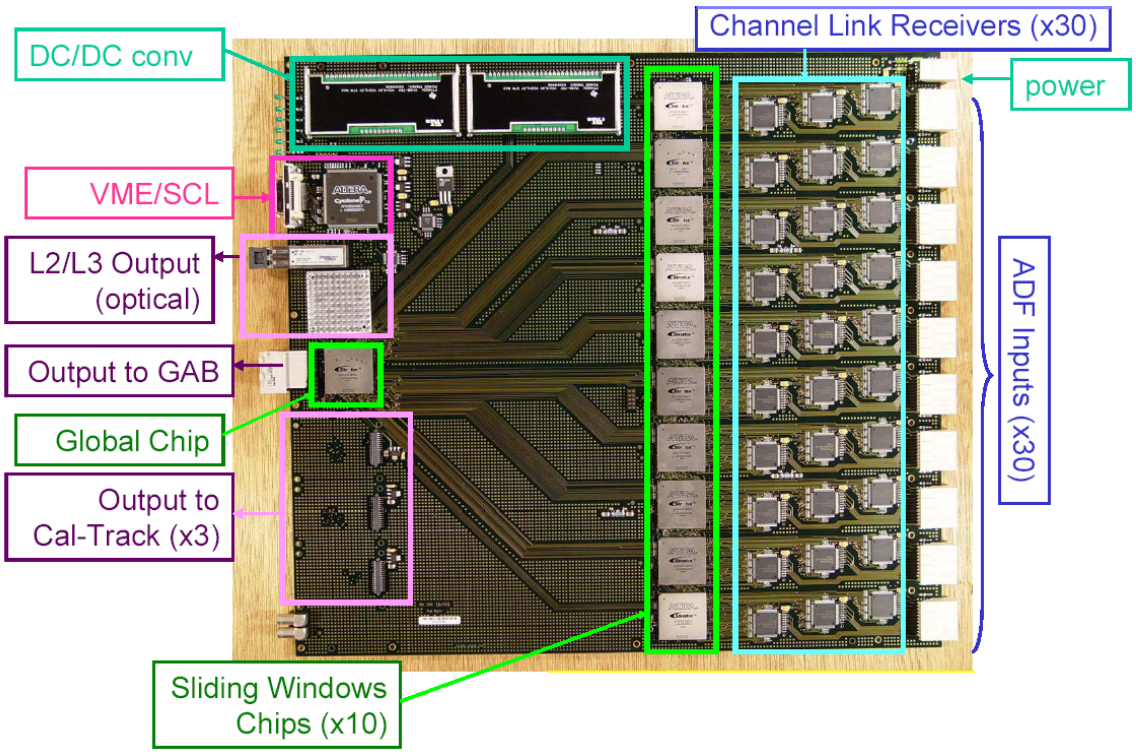

Figure 10: Trigger Algorithm Board (TAB) prototype which receives inputs from 30 different ADF cards and 480 TTs.

TAB Board #	1			2			3			4		
Trigger Phi	29-32	1-4	5-8	1-4	5-8	9-12	5-8	9-12	13-16	9-12	13-16	17-20
SW Chip vs Trigger Eta	A	B	C	A	B	C	A	B	C	A	B	C
1_____-20 –17	80	73	74	73	74	75	74	75	76	75	76	77
2_____-16 -13	64	57	58	57	58	59	58	59	60	59	60	61
3_____-12 -9	48	41	42	41	42	43	42	43	44	43	44	45
4_____-8 -5	32	25	26	25	26	27	26	27	28	27	28	29
5_____-4 -1	16	9	10	9	10	11	10	11	12	11	12	13
6_____1 4	8	1	2	1	2	3	2	3	4	3	4	5
7_____5 8	24	17	18	17	18	19	18	19	20	19	20	21
8_____9 12	40	33	34	33	34	35	34	35	36	35	36	37
9_____13 16	56	49	50	49	50	51	50	51	52	51	52	53
10_____17 20	72	65	66	65	66	67	66	67	68	67	68	69

TAB Board #	5			6			7			8		
Trigger Phi	13 16	17 20	21 24	17 20	21 24	25 28	21 24	25 28	29 32	25 28	29 32	1 4
SW Chip # vs Trigger Eta	A	B	C	A	B	C	A	B	C	A	B	C
1_____-20 -17	76	77	78	77	78	79	78	79	80	79	80	73
2_____-16 -13	60	61	62	61	62	63	62	63	64	63	64	57
3_____-12 -9	44	45	46	45	46	47	46	47	48	47	48	41
4_____-8 -5	28	29	30	29	30	31	30	31	32	31	32	25
5_____-4 -1	12	13	14	13	14	15	14	15	16	15	16	9
6_____1 4	4	5	6	5	6	7	6	7	8	7	8	1
7_____5 8	20	21	22	21	22	23	22	23	24	23	24	17
8_____9 12	36	37	38	37	38	39	38	39	40	39	40	33
9_____13 16	52	53	54	53	54	55	54	55	56	55	56	49
10_____17 20	68	69	70	69	70	71	70	71	72	71	72	65

Figure 11: ADF output distribution to TAB per ADF board, per SW chip. Each ADF card is numbered from 1 to 80 and appears three times in the above table. The color scheme distinguishes in which ADF crate and rack the ADF card is located.

BLS to ADF Connection Mapping

Patch Panel (PP)

The patch panels are design to link the BLS “Blue cables” to the ADF inputs.

They have three constituents. The Patch Panel Cards (PPC), the Pleated Foil Cables (PFC) and the Paddle Cards (PC).

Patch Panel Card (PPD)

The Patch Panel Cards are where the BLS cables are connected. There are two Patch Panel Cards per module Figure 12. Each rack has 4 of these modules. Each PPC has 2 Pleated Foil connectors (output) in the top and 16 BLS connectors behind them (input). These cards are located in the front of the crate and the connectors described are located in the inner face of the card (Figure 12a). In the bottom there are testing terminals located in the front face of the card (Figure 12b). In total there are 80 PPC in 40 modules.

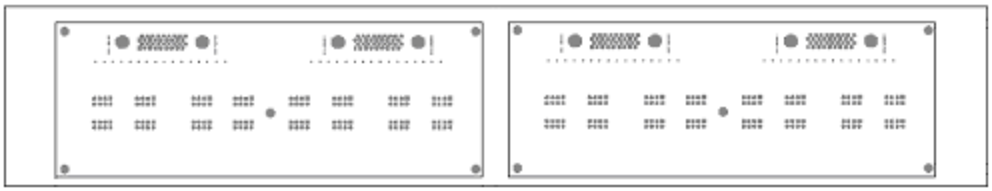

Figure 12a: Back of the Patch Panel Card module.

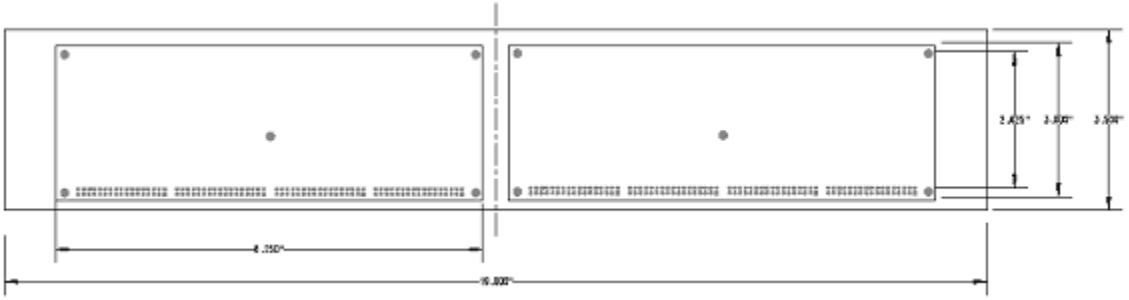

Figure 12b: Front of the Patch Panel Card module.

Paddle Card (PC)

Each Paddle Card is connected with a Patch Panel Card using two Pleated Foil Cables (input from two pleated foil connectors) Figure 12, and each PC is connected in the ADF backplane Figure 13 via ERNI connector (output).

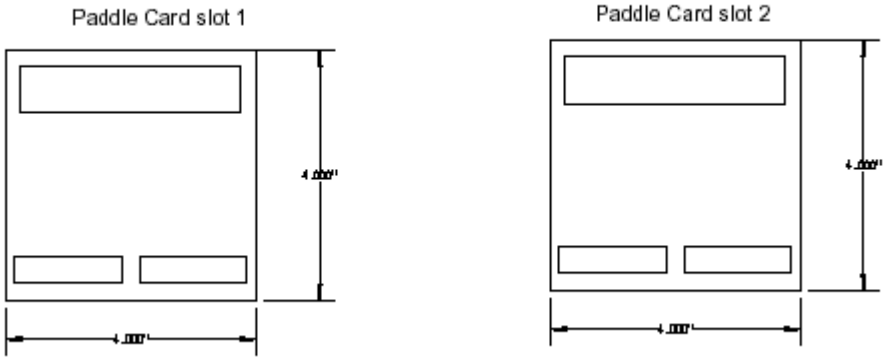

Figure 12: Two Paddle Cards are linked with a single Patch Panel Card module; it means each Paddle Card is connected with a single Patch Panel Card via two Pleated Foil Cables.

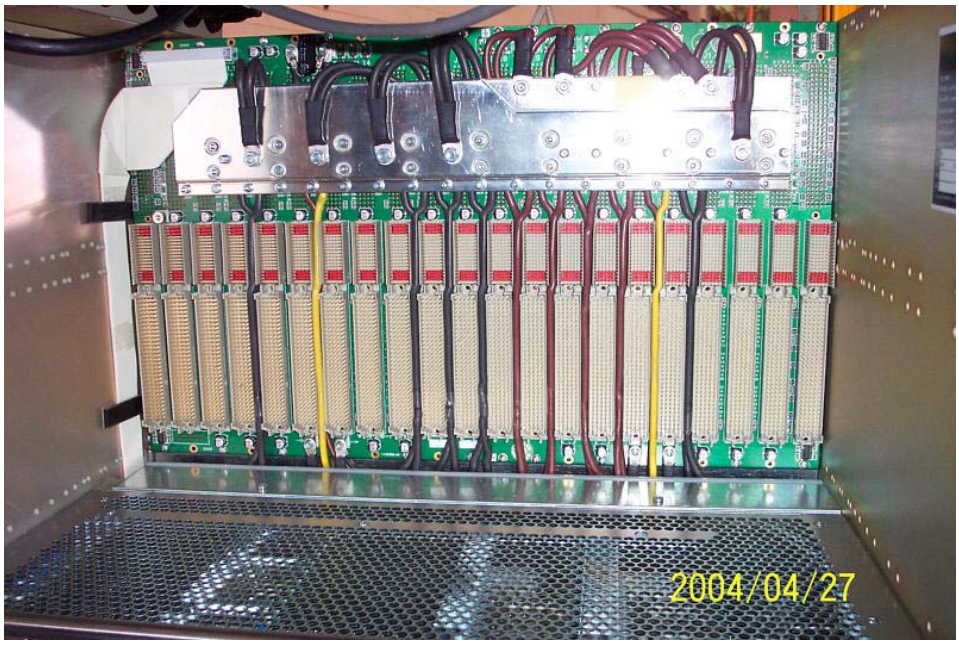

Figure 13: ADF backplane.

In total there are 80 Paddle Cards; each one is connected with a single ADF card.

Pleated foil cable (PFC)

The 3M - Pleated Foil Cables (FERMILAB customized) Figure 14 are the cables which link the Patch Panel Cards with the Paddle Cards. There are 160 of them.

Figure 14: 9.5 feet pleated foil cables.

Appendix – Cable Mapping Spreadsheet

The spreadsheet Cables_RunIIb.xls provides a detailed mapping of each existing BLS cable in the current L1 trigger and it shows in which ADF channel is going to be connected.

Run I

In the first tag named "By ADF Board" it is shown the calorimeter BLS coordinates for each BLS connector (columns A to G)[1]. Next to that it is shown the BLS location (rack, crate and slot, columns H to J). In the following two columns are the trigger tower coordinates (columns L and M). Columns N to Q have the current L1 rack, crate, slot and connector for each cable. Column R is the physics location in the calorimeter.

In columns S, T and U we label with a number each ribbon and bundle in such a way we can easily check we do not split them.

ADF I/O.

In columns W to Z and AA to AF we assign each BLS connector to an ADF rack, crate, board and channel and also we show the corresponding ADF output.

Patch Panel

Patch Panel Card

From the column AH to AT we show how each BLS pin is connected with the Pleated Foil Cable. This information was taken from the schematic for the PPC Figure 15.

In the column AH we label the PP modules (serial number). There are 40 of them.

In the column AI we show which PPC (1 or 2).

AJ has the rack location.

AK has the connector on the PPC where the BLS cable is connected.

Columns AL to AO have the pins with signal of the BLS cable. Pins 1, 3, 5, 7 = E+,E–,H+,H–. In columns AP to AU we show how these pins are connected with the Pleated Foil connector (following left to right order). An also the diagnostic pick of pins on columns AV to AZ.

[1] The eta convention used starts in 0; because of this we add two extra columns with eta starting in 1 (columns F and G)

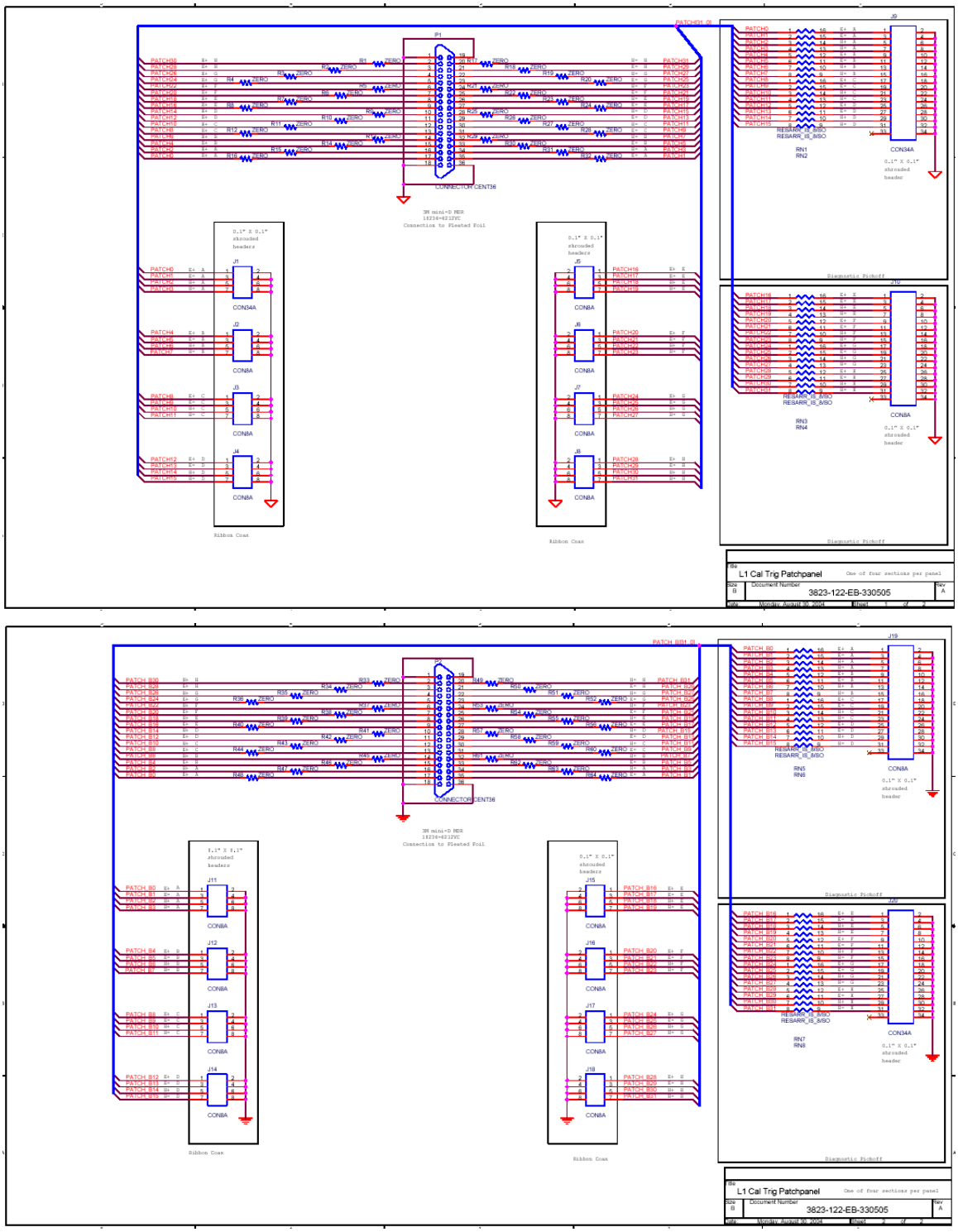

Figure 15: Schematic of the Patch Panel Card.

Pleated Foil Cable

In columns BB to BP we show the Pleated Foil Cable labeling. The lines are separated using "/". In this way first line has the PFC number (1 to 160); the second line has the source location (rack, PP, PPC and connector) and the third has the destination location (rack, PC and connector).

Paddle Card

From column BR to CC we follow the paddle card schematic Figure 16 for each BLS pin.

BR has the PC number (1 to 80)

BS has the rack location.

From BT to BX have the PFC number and pins.

From BZ to CC have the ERNI pins distribution (input for the ADF card). In this point we have to be aware; when we use J1 B (column B on connector J1) on VME-64x convention means column A. In the same way column D on connector J1 (J1 D) on VME-64x convention means column C.

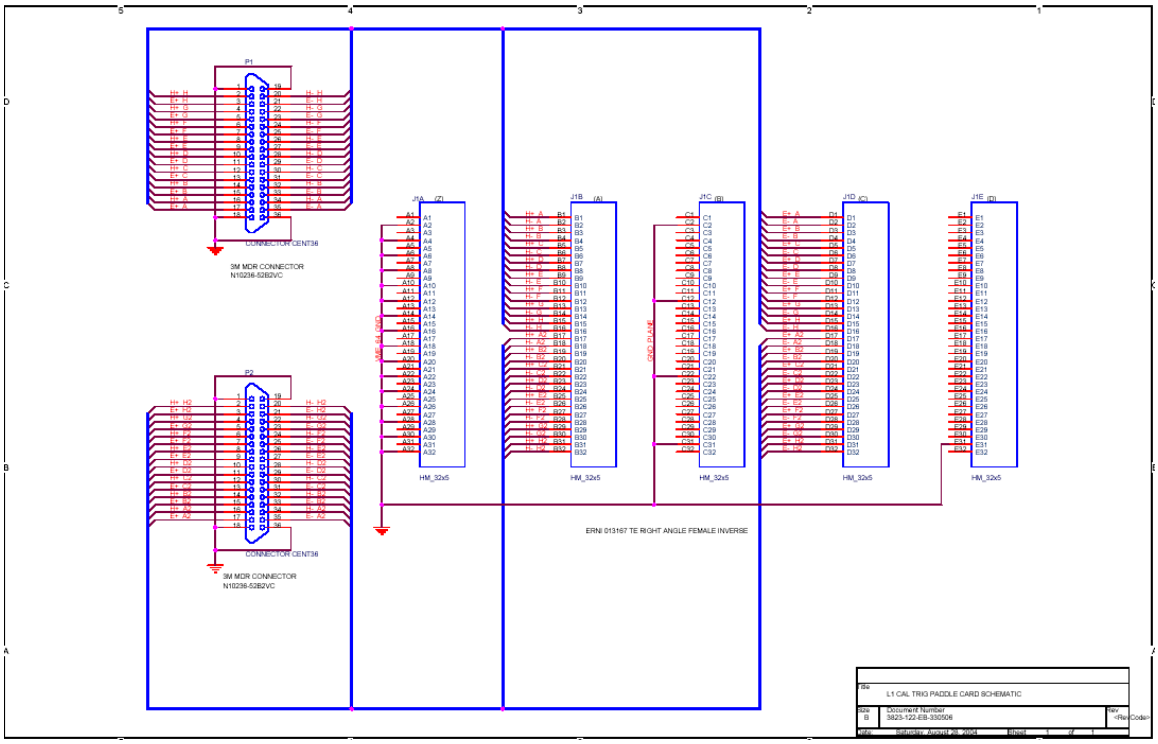

Figure 16: Paddle Card Schematic. In the J1 connector we use the convention A (Ground), B, C, D, E to name the columns where the VME-64x convention is Z (Ground), A, B, C, D.

BLS labeling

In columns CE to CX we define a new label for the BLS cables. The lines are separated using "/". In this way the first line has the BLS cable number (1 to 1280); the second line has the source location (rack, crate, slot plus TTeta anTTphi) and the third has the destination location (rack, PP, PPC and connector).

Summarizing, in each row is shown a detailed end-to-end description for a given BLS connector pin by pin.

In the second tag named "TAB" is given a draft of the connection between the ADF output and the TAB input. Each ADF board is connected with three TAB inputs in different SW chips. Also each TAB SW chip offers an input for three ADF outputs. In the fifth tag named "SW INPUTS FROM ADF BOARDS" an inversed mapping is showed. It's shown which three SW chips are linked with a given ADF board output. The same thing is shown in the first tag columns W to AF.

In the third tag named "ADF ETA&PHI DIST" there is a chart showing the eta&phi distribution for the ADF boards; and also the current eta&phi distribution per rack.

In the forth tag named "ADF OUTPUT ON SW CHIPS" it is shown the eta&phi distribution in the tab board and how phi is overlapped in the TAB boards.

Acknowledgements

The necessary documentation and pictures were provided for Hal Evans (Columbia University).
http://www.nevis.columbia.edu/~evans/l1cal/hardware/hardware.html
Also mention Dan Edmunds, Phillip Laurens and Denis Calvet.

References

[1] "D0 RUN IIB UPGRADE TECHNICAL DESIGN REPORT".
D0 Collaboration, FERMILAB-PUB-02-327-E, Dec 2002.

[2] Figures 1a-b were borrowed with permission from the Michigan State University Run IIa L1 Cal Trigger web page, maintained by Dan Edmunds and Philippe Laurens: http://www.pa.msu.edu/hep/d0/l1/cal_trig/.

[3] “Cables that Run from the Existing BLS Trigger Tower Pickoff Signal Cables to ADF Backplane”, D. Edmunds (10 Apr 2004)
http://www.pa.msu.edu/hep/d0/ftp/run2b/l1cal/hardware/adf_2/general/bls_to_adf_backplane_extension_cables.txt

[4] “Cabling in the Run IIb L1Cal Trigger”
http://www.nevis.columbia.edu/~evans/l1cal/hardware/cabling/adf_to_tab_cable_map.html#cablediag

[5] For a description of the calorimeter layout, layers, and towers, see D0 Note 774, “Calorimeter Addressing - Version 1.1”, Jim Linnemann (11/7/88).

The full description of the current BLS cable runs is provided in:
[6] “Central BLS Card to Calorimeter Trigger Front-End Card” Hal Evans (6/6/90)
(http://www.pa.msu.edu/hep/d0/ftp/run1/l1/caltrig/cabling/central_bls_card_to_ctfe_card.txt)

[7] “End Cap BLS Card To Calorimeter Trigger Front-End Card” Hal Evans (6/6/90)
(http://www.pa.msu.edu/hep/d0/ftp/run1/l1/caltrig/cabling/end_cap_bls_card_to_ctfe_card.txt)

[8] A full map can be found on the following spread sheet:
(http://www2.uic.edu/~mcamuy2/trigger/Cables_BLS_CTFE_New_Conf_A05.xls)